REMARKS

Claims 1 - 17 are pending in the application.

Claims 1-7, and 9-17 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Hagersten et al. (U.S. Publication No. 2002/0019921) (hereinafter "Hagersten (2002/0019921)"). Applicant respectfully traverses this rejection and respectfully requests reconsideration in view of the following remarks.

Claim 8 stands rejected under 35 U.S.C. §103(a) as being unpatentable over Hagersten (2002/0019921) in view of Arimilli et al. (U.S. Publication No. 2002/0112124) (hereinafter "Arimilli"). Applicant respectfully traverses this rejection.

Applicant's claim 1 recites a system comprising in pertinent part,

> "within that active device and to responsively output a global address identifying a coherency unit, wherein a portion of the global address identifies a translation function;
>
> wherein a memory subsystem included in the node is configured to perform the translation function **identified by the portion of the global address on an additional portion of the global address** in order to obtain a local physical address of the coherency unit;
>
> wherein each active device included in the node is configured to use the portion of the global address identifying the translation function when determining whether a local copy of the coherency unit is currently stored in a cache associated with that active device."
>
> (Emphasis added)

The Examiner asserts Hagersten teaches the above limitations. Applicant respectfully disagrees with the Examiner's characterization of Hagersten. First, the Examiner has rejected claims 1-7, and 9-17 under 35 U.S.C. §103(a). However, the Examiner has not discussed what is not taught by Hagersten, or what is obvious. Instead,

in the Detailed Action, the Examiner appears to be asserting Hagersten teaches each limitation of the claims. In addition, Applicant has tried (to no avail) to locate any of the passages in Hagersten (2002/0019921) that are referenced by the Examiner. Applicant cannot find any of the referenced passages in Hagersten. Specifically, the Examiner refers to FIG. 3B, and reference designator #312A MMU of Hagersten. However, FIG. 3B does not exist in Hagersten, and the MMU's are designated 76A-76B in FIG. 2.

Applicant submits Hagersten is directed toward translating global addresses to local addresses using tables, wherein in the Summary paragraph [0017] Hagersten discloses

> "Broadly speaking the present invention contemplates a look-up table configured to store and output data corresponding to input addresses. The lookup table includes a plurality of entries for storing the data and a look-up address circuit. The look-up address circuit is configured to receive the input address and includes a first index function circuit and a second index function circuit. The first index function circuit is configured to convert a first input address to a primary look-up address that corresponds to the first input address, wherein a primary entry of the plurality of entries is addressed by the primary look-up address. The second index function circuit is configured to convert the first input address to a secondary look-up address that corresponds to the first input address, wherein a secondary entry of the plurality of entries is addressed by the secondary look-up address. The look-up table is configured to store a first datum to the primary entry if the primary entry is available and to store the first datum to the secondary entry if the primary entry is unavailable. If the primary entry and the secondary entry are unavailable, the look-up table is configured to move a second datum stored in the primary entry (or secondary entry) to an alternate entry for the second datum and to store the first datum to the primary (or secondary entry) entry." (Emphasis added)

From the foregoing, it appears Hagersten teaches translation of global addresses to local addresses using look-up tables and indexing functions that are converted to secondary addresses by index function circuits. This is clearly different than the limitations recited in Applicant's claim 1. Specifically, Applicant submits Hagersten does not teach or suggest "a portion of the global address identifies a translation function." In addition, Hagersten does not teach or suggest "wherein a memory subsystem included in the node is configured to perform the translation function

identified by the portion of the global address on an additional portion of the global address in order to obtain a local physical address of the coherency unit." Finally, Hagersten does not teach or suggest "wherein each active device included in the node is configured to use the portion of the global address identifying the translation function when determining whether a local copy of the coherency unit is currently stored in a cache associated with that active device," as recited in Applicant's claim 1.

Arimilli is not relied upon by the Examiner for global address translation.

Accordingly, Applicant submits claim 1, along with its dependent claims patentably distinguishes over Hagersten, and over Hagersten in view of Arimilli for the reasons given above. In addition, Applicant's claim 9 recites features that are similar to the features recited in claim 1. Thus, for at least the reasons given above, Applicant submits claim 9, along with its dependent claims, patentably distinguishes over Hagersten.

CONCLUSION

Applicant submits the application is in condition for allowance, and an early notice to that effect is requested.

If any fees are due, the Commissioner is authorized to charge said fees to Meyertons, Hood, Kivlin, Kowert, & Goetzel, P.C. Deposit Account No. 501505/5181-98801/BNK.

Respectfully submitted,

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